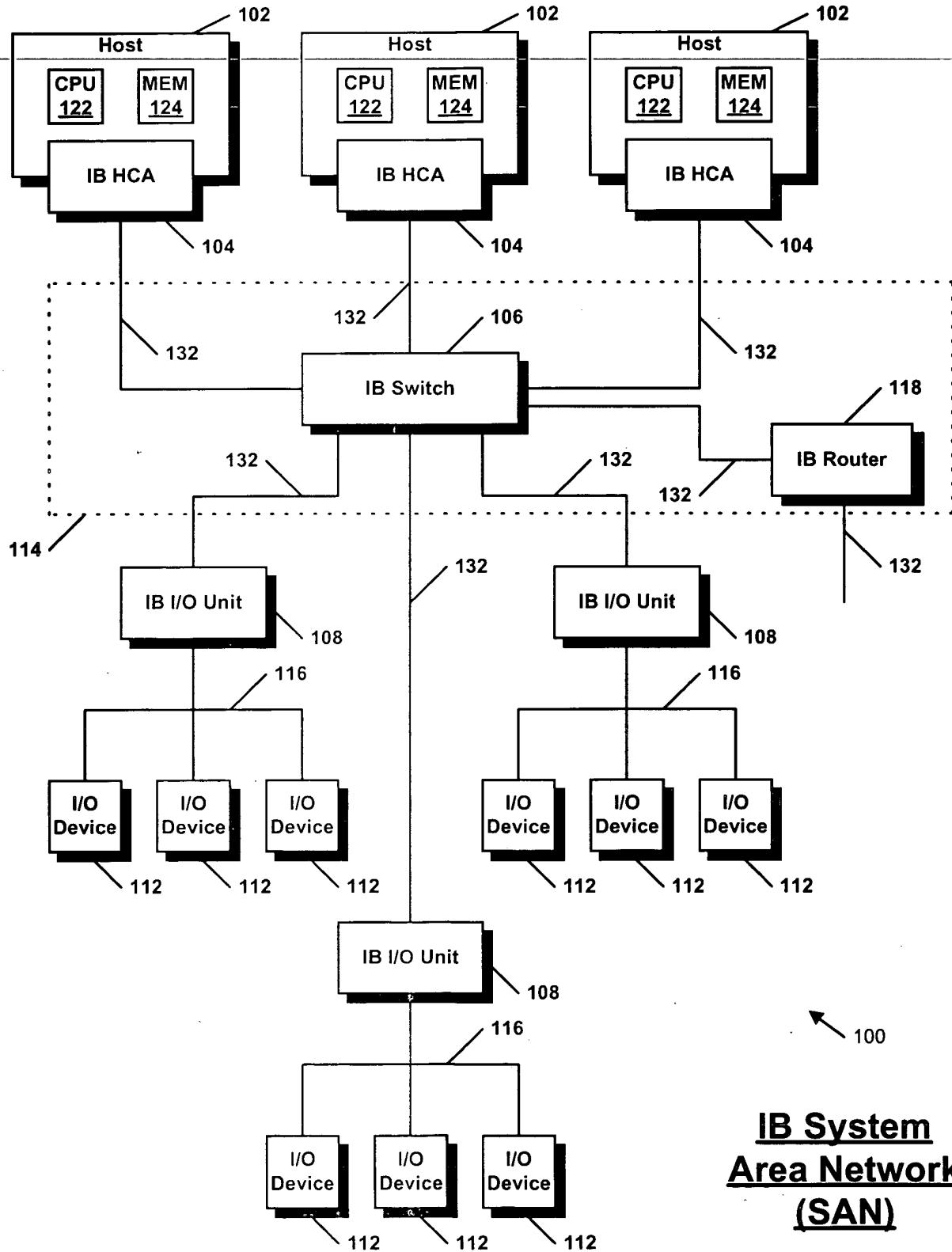
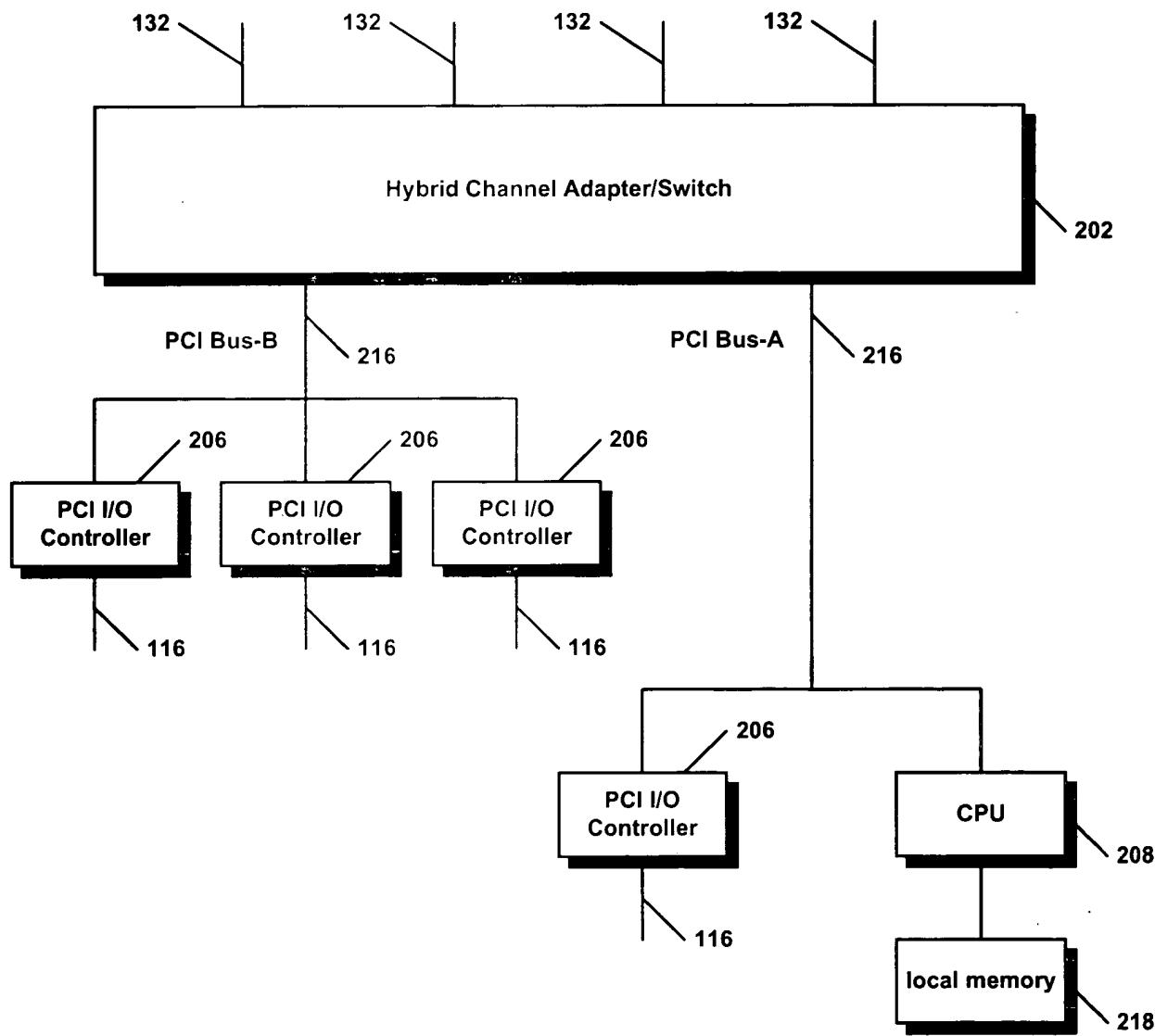


FIG. 1



IB System
Area Network
(SAN)

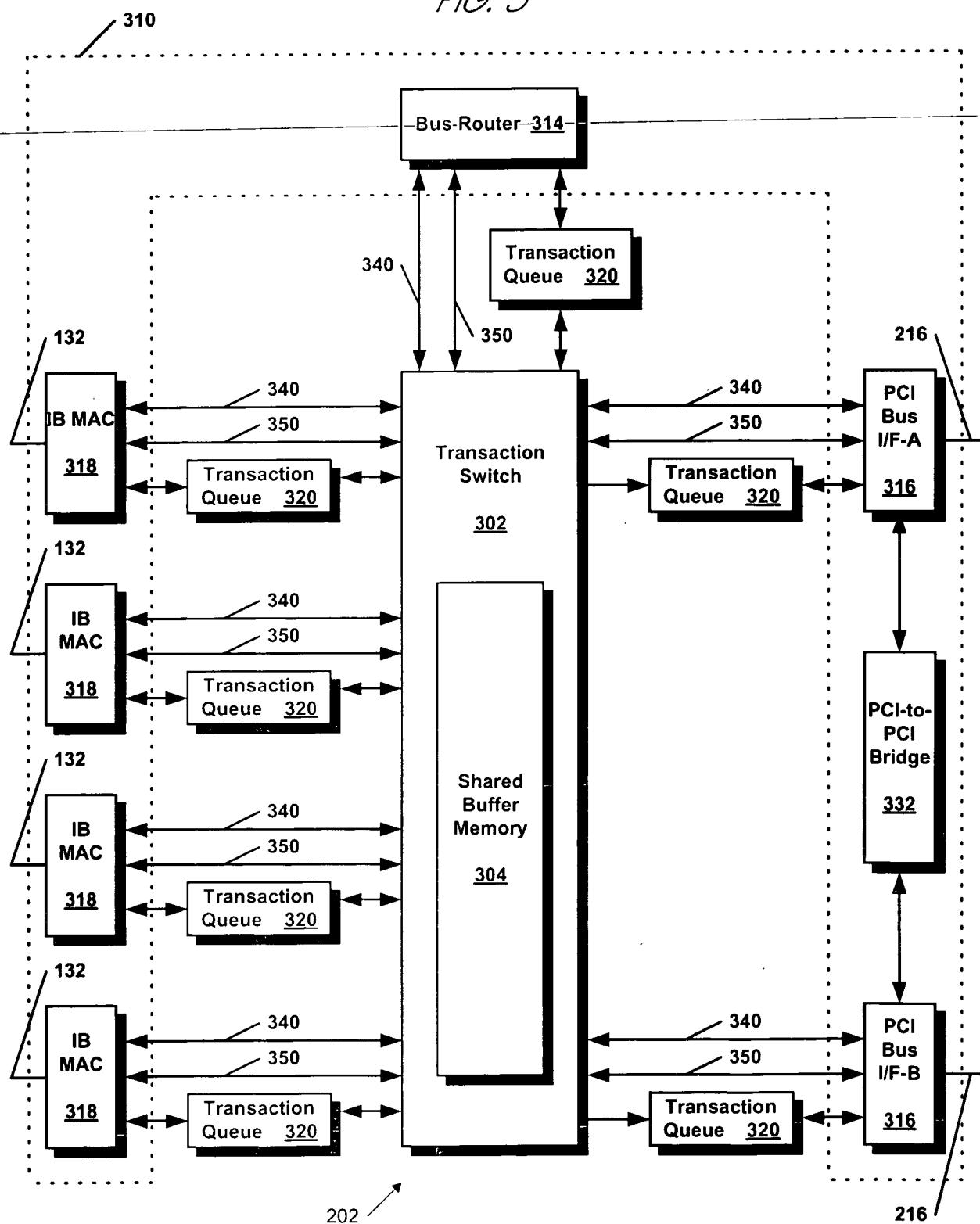
FIG. 2



IB Hybrid Channel Adapter/Switch

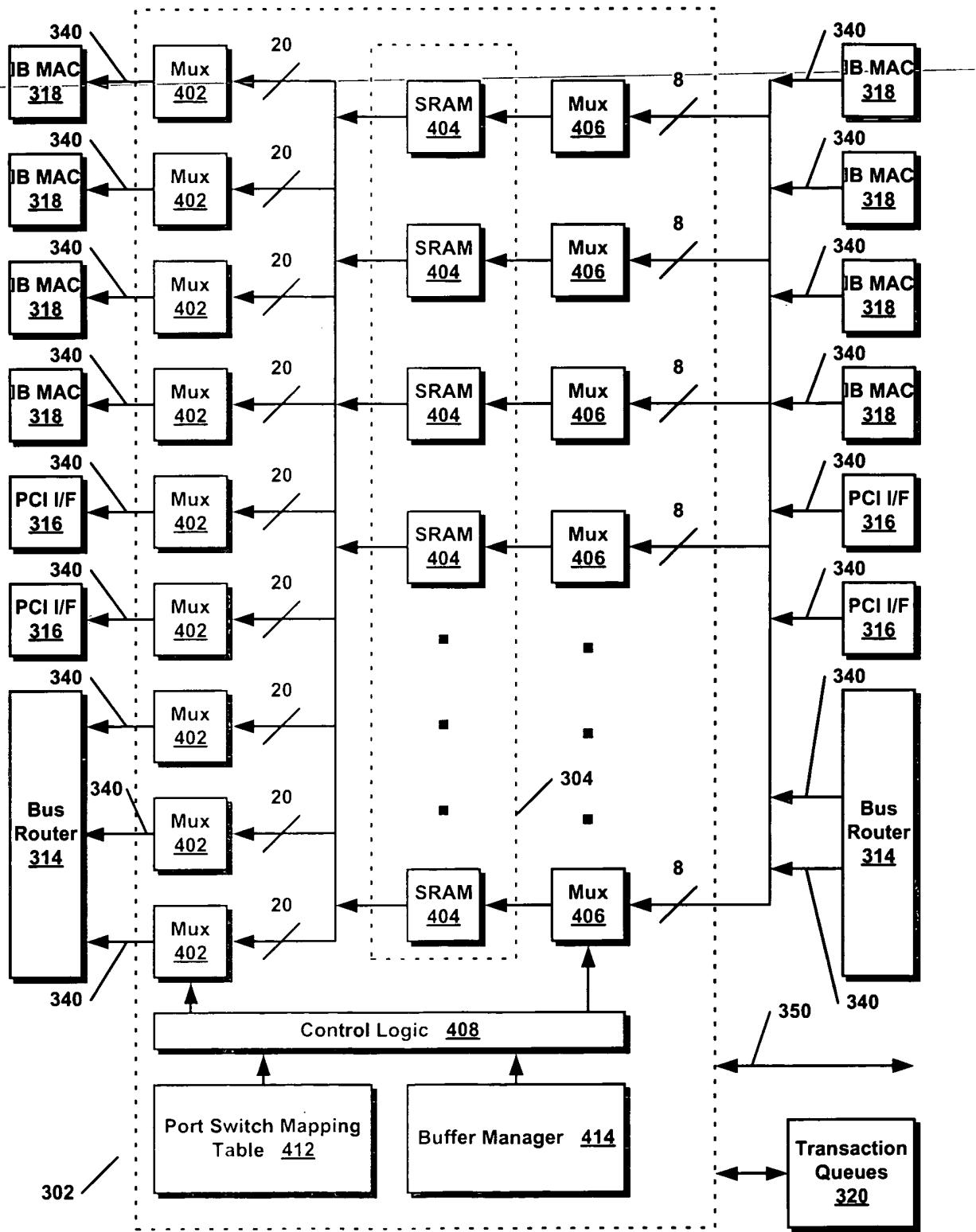
FIG. 3

1020220 = 8002T360



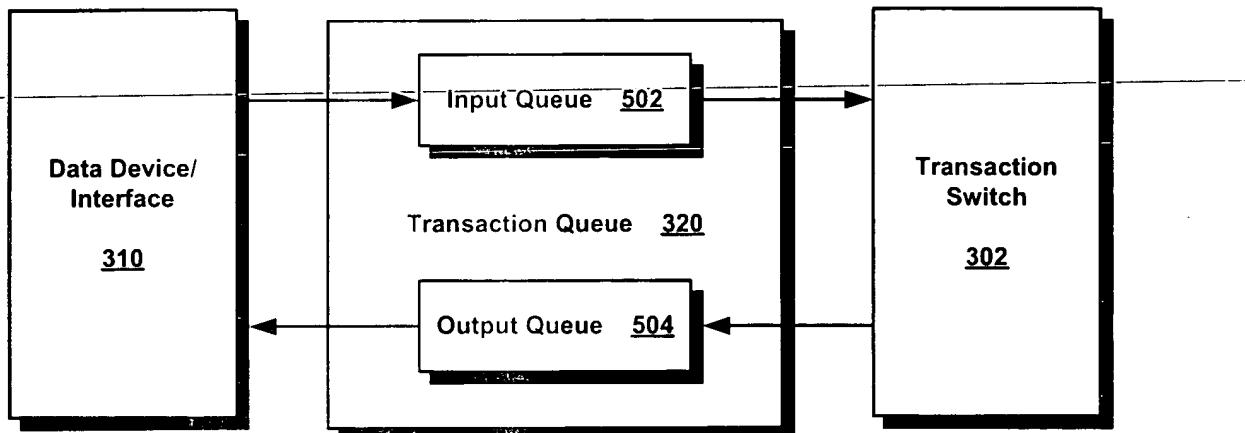
IB Hybrid CA/Switch with Transaction Switch and Shared Buffer Memory

FIG. 4



Transaction Switch Data Paths

FIG. 5



Transaction Queues

FIG. 6

DLID <u>602</u>	Frame Error <u>604</u>	LNH <u>606</u>	Destination QP <u>608</u>	Packet Length <u>612</u>	VL <u>614</u>	Buffer Address <u>616</u>
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MAC Input Queue Entry

600 →

FIG. 7

Tag <u>702</u>	PCI Address/Port <u>704</u>	Length <u>706</u>	Offset <u>708</u>	VL <u>712</u>	Type <u>714</u>	Buffer Address <u>716</u>
-------------------	--------------------------------	----------------------	----------------------	------------------	--------------------	------------------------------

Bus Router Input Queue Entry

700 →

FIG. 8

Not Raw <u>802</u>	Tag <u>804</u>	Packet Length <u>806</u>	VL <u>808</u>	Buffer Address <u>812</u>
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MAC Output Queue Entry

← 800

FIG. 9

Port <u>902</u>	Frame Error <u>904</u>	LNH <u>906</u>	Destination QP <u>908</u>	Length <u>912</u>	VL <u>914</u>	Buffer Address <u>916</u>
--------------------	---------------------------	-------------------	------------------------------	----------------------	------------------	------------------------------

Bus Router Output Queue Entry

← 900

FIG. 10

Tag <u>1002</u>	PCI Address <u>1004</u>	Length <u>1006</u>	Offset <u>1008</u>	PCI Type <u>1012</u>	Buffer Address <u>1014</u>
--------------------	----------------------------	-----------------------	-----------------------	-------------------------	-------------------------------

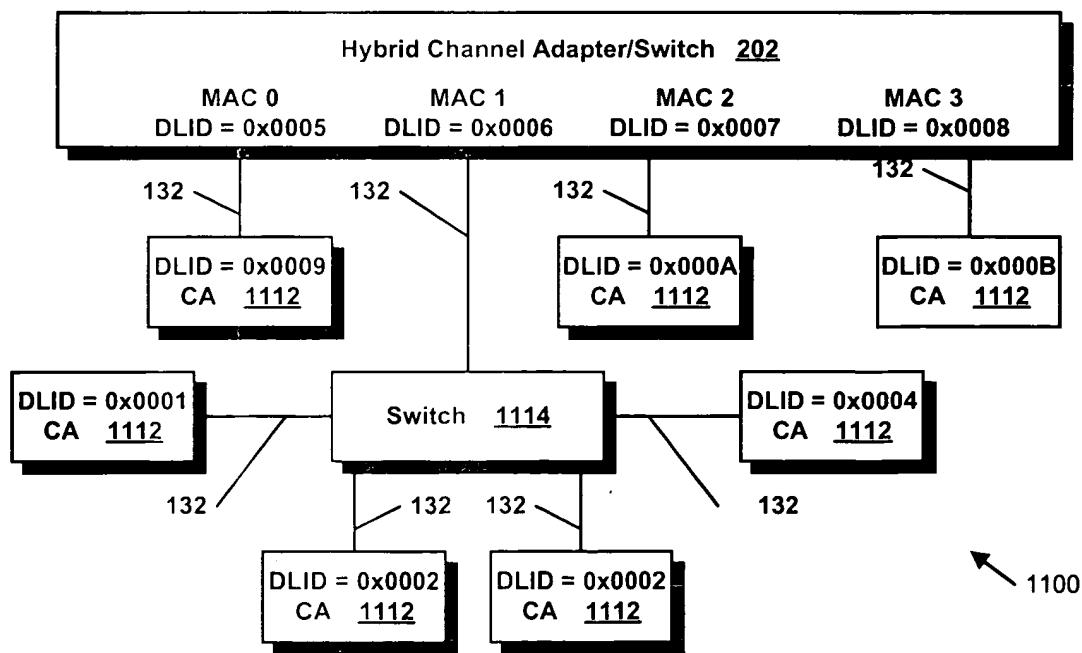
PCI Output Queue Entry

← 1000

FIG. 11

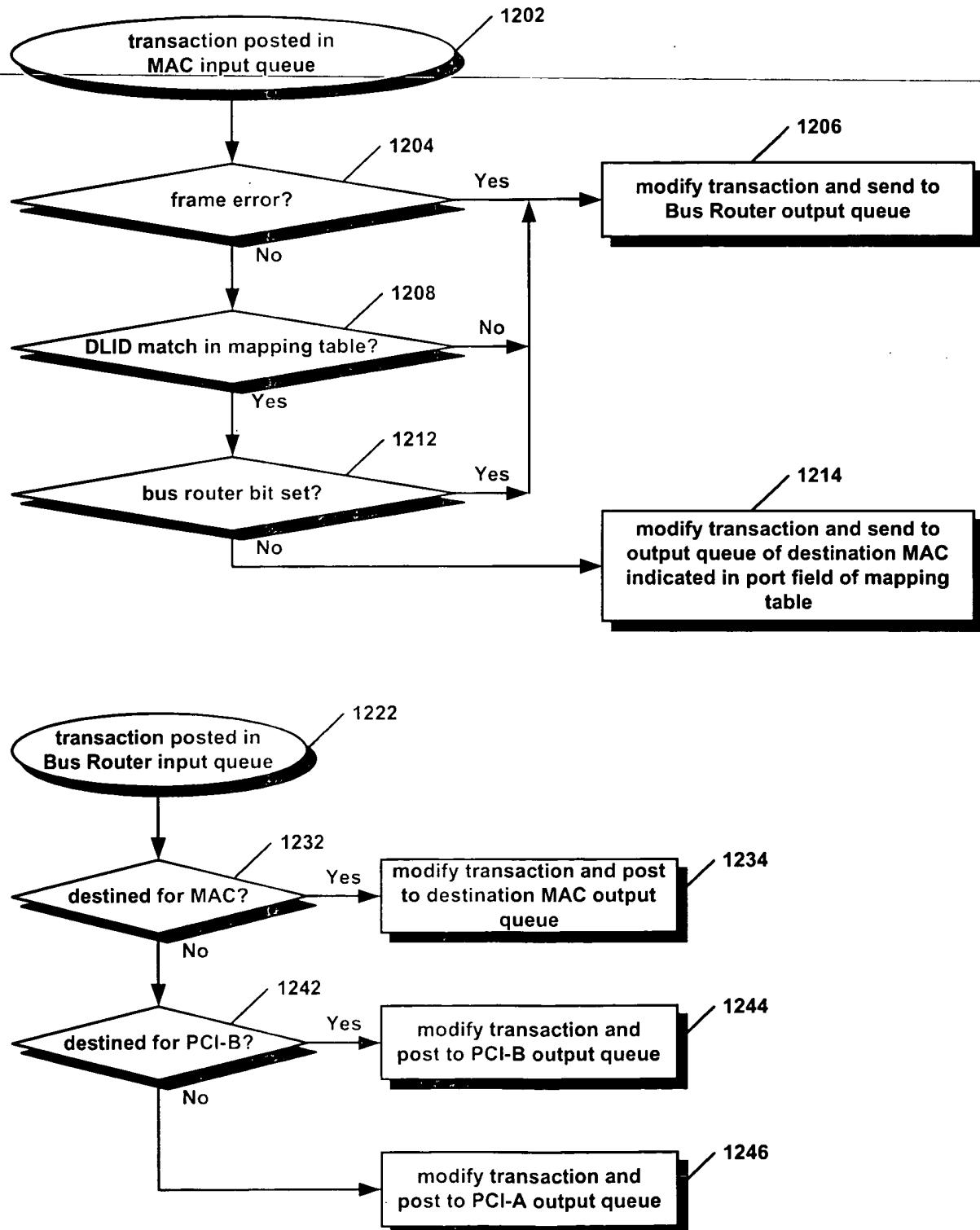
Bus Router <u>1102</u>		Port <u>1104</u>	DLID	Valid
0	1	0	<u>1106</u>	<u>1108</u>
0	1	0	0x0005	1
1	1	1	0x0006	1
2	1	2	0x0007	1
3	1	3	0x0008	1
4	0	1	0x0001	1
5	0	1	0x0002	1
6	0	1	0x0003	1
7	0	1	0x0004	1
8	0	0	0x0009	1
9	0	2	0x000A	1
10	0	3	0x000B	1
11	0	2	-	0
12	0	1	-	0
13	0	3	-	0
14	0	2	-	0
15	0	2	0x0007	1

412 →



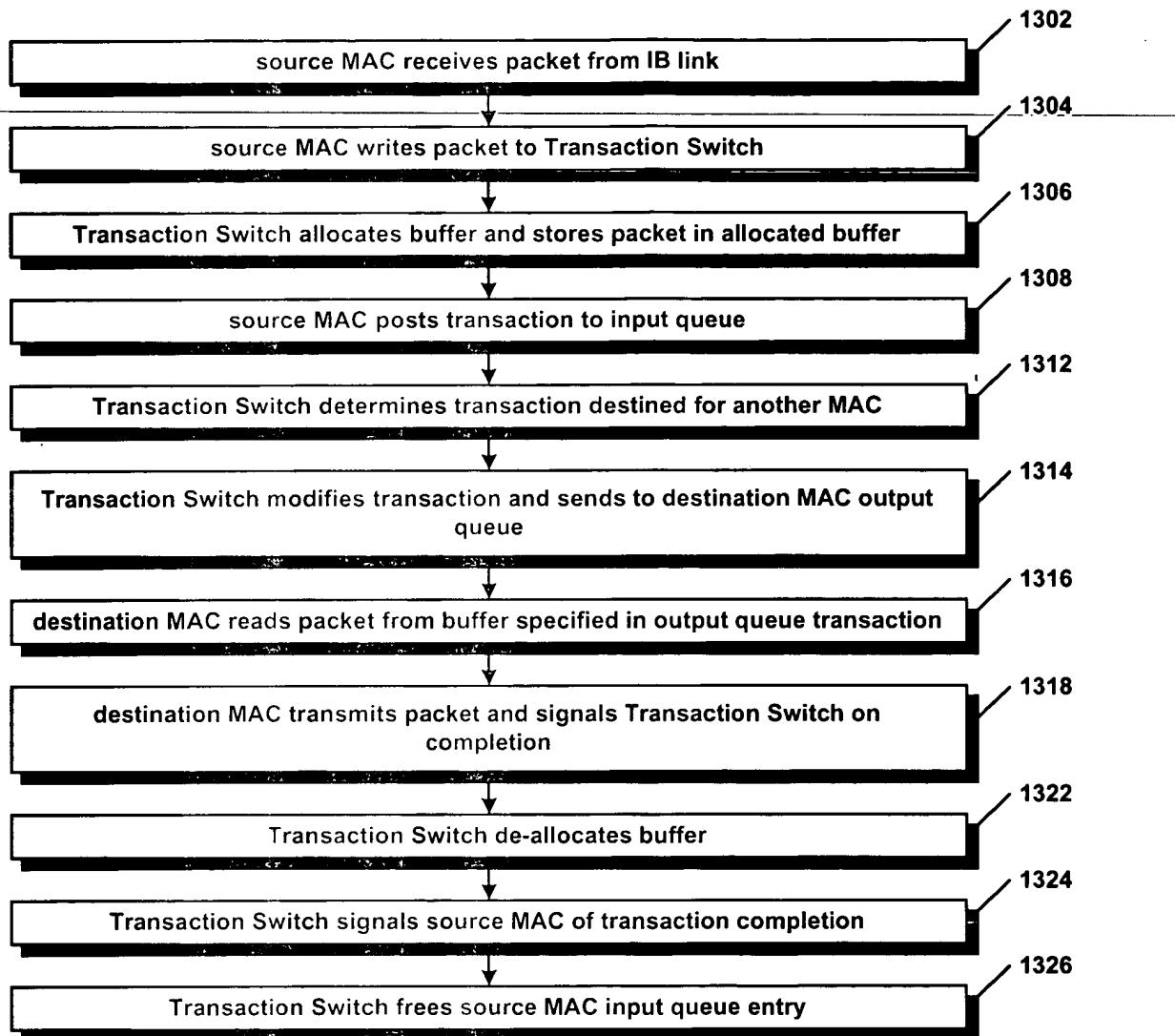
Port Switch Mapping Table in Example Network

FIG. 12



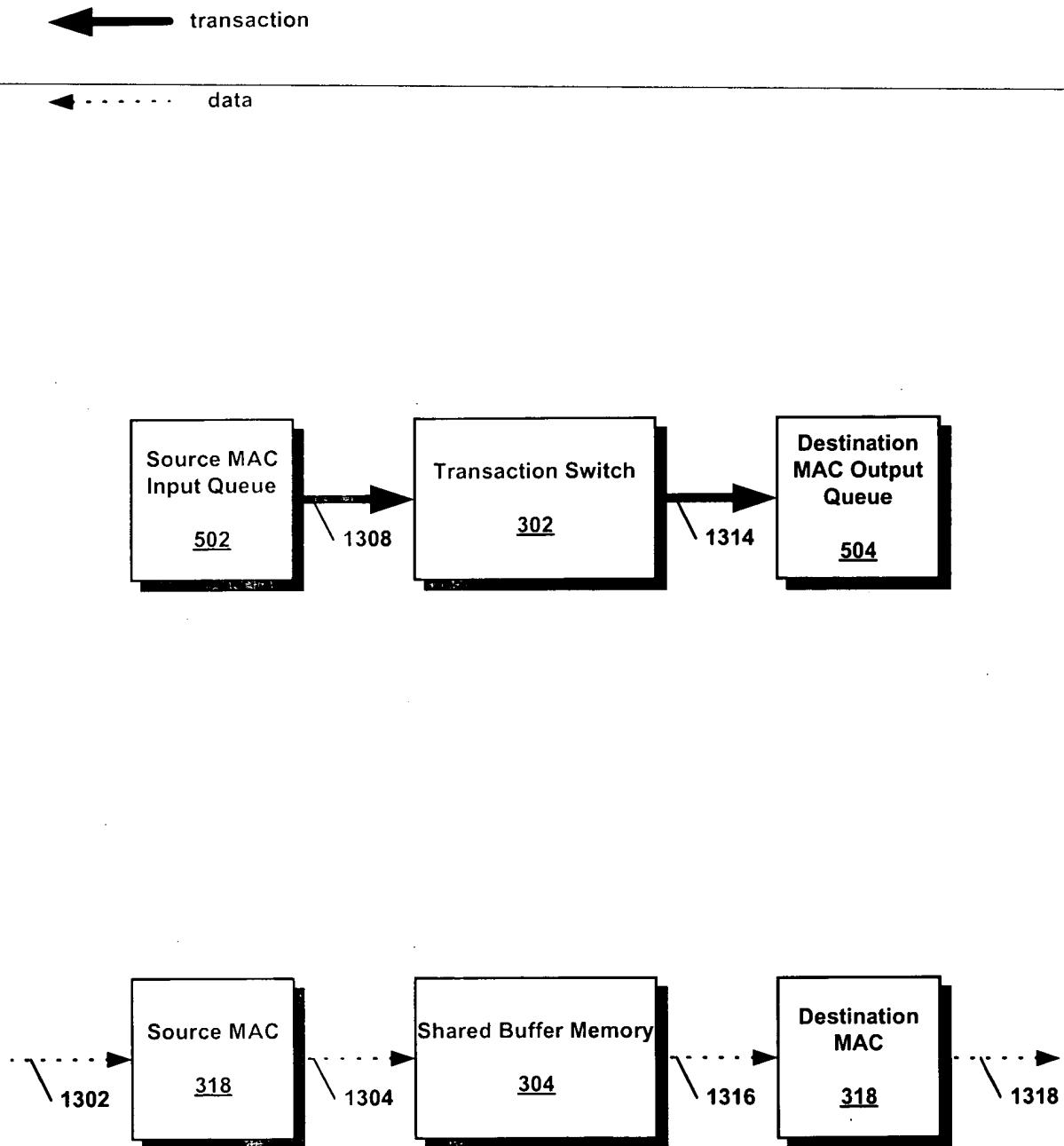
Transaction Switching

FIG. 13a



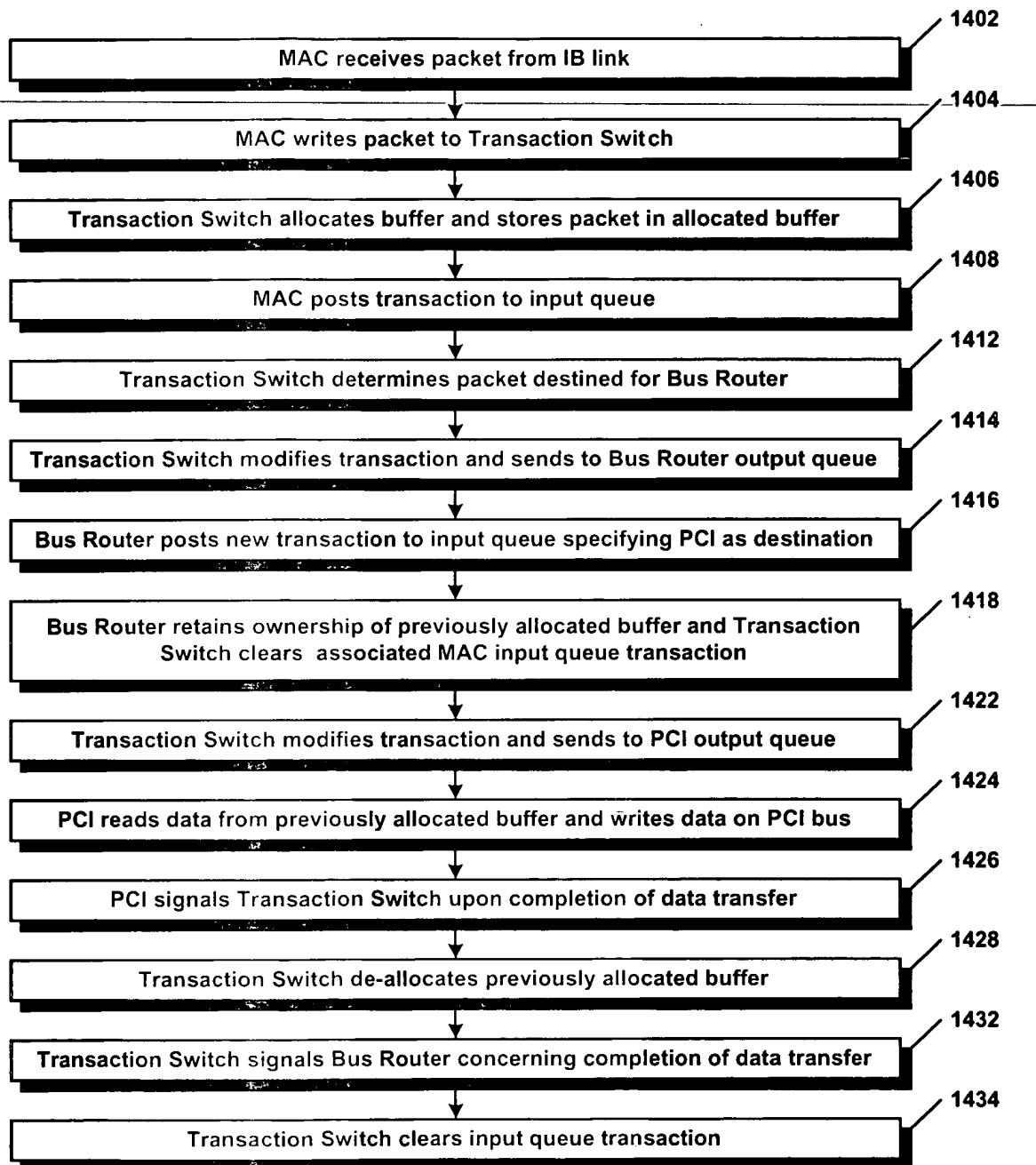
Packet Switching Operation

FIG. 13b



Packet Switching Operation

FIG. 14a



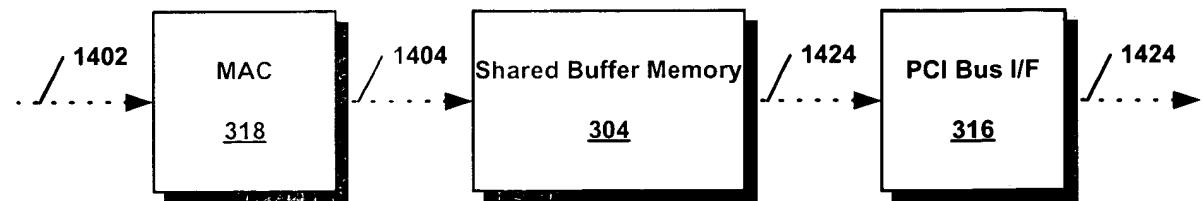
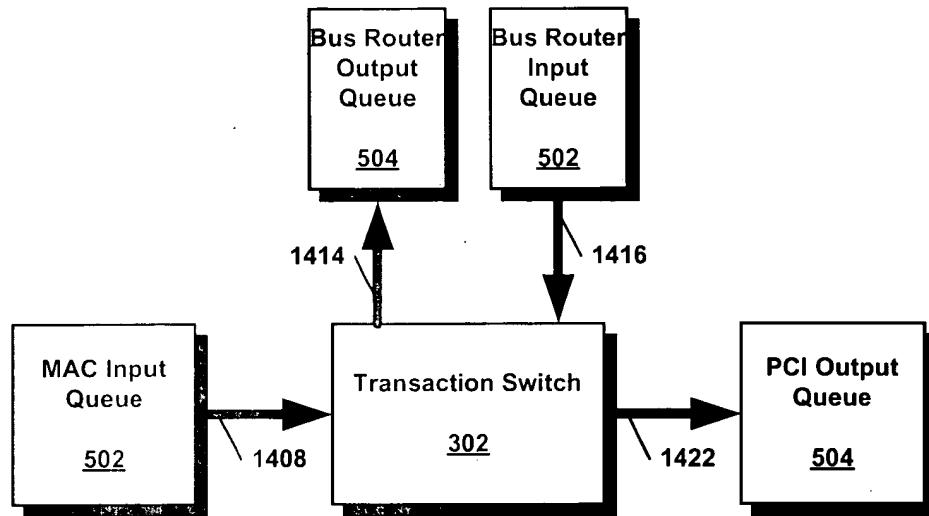
Packetized Data to Addressed Data Operation

FIG. 14b

TRANSMITTED BY DRAFTS

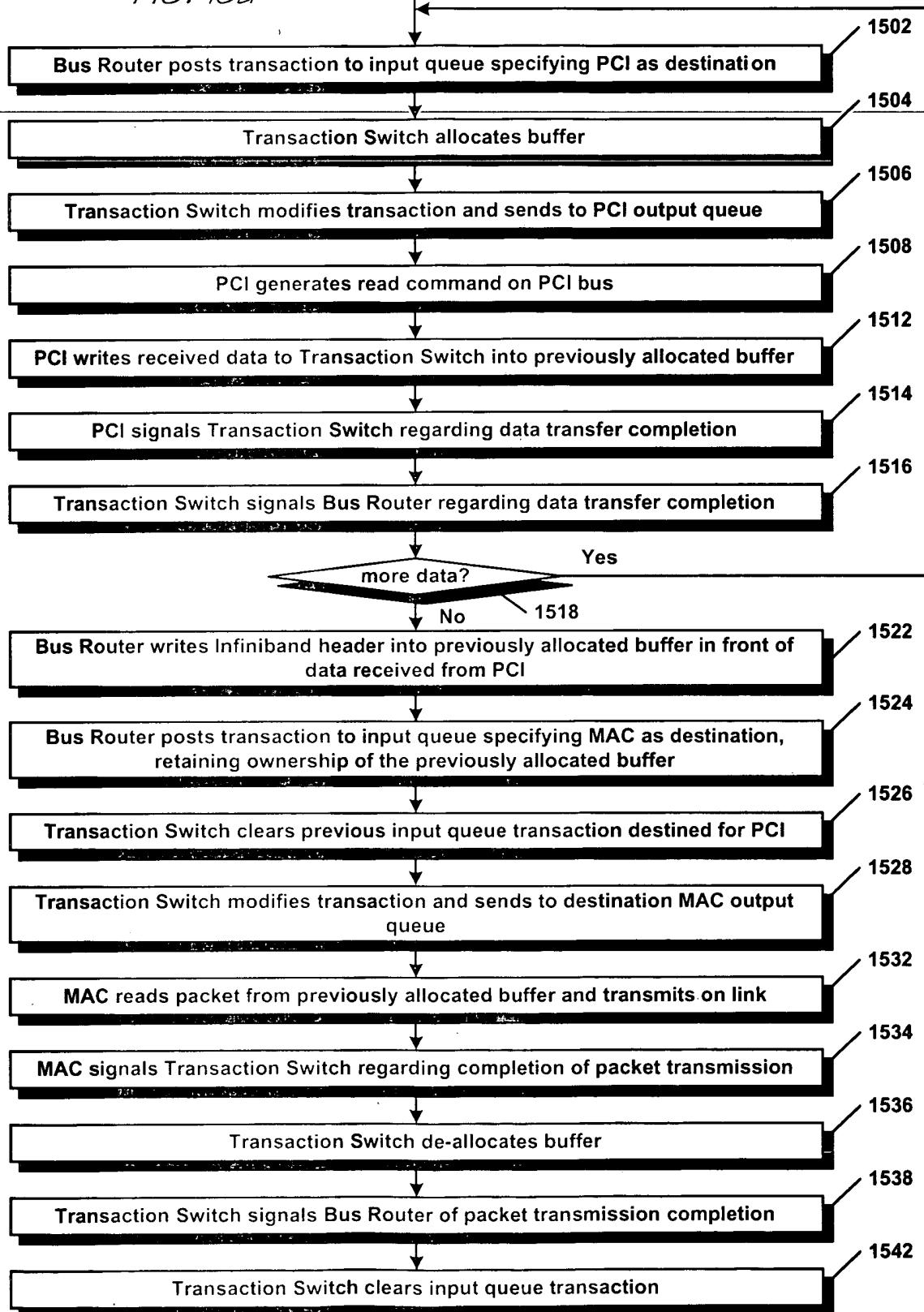
← transaction

← ···· data



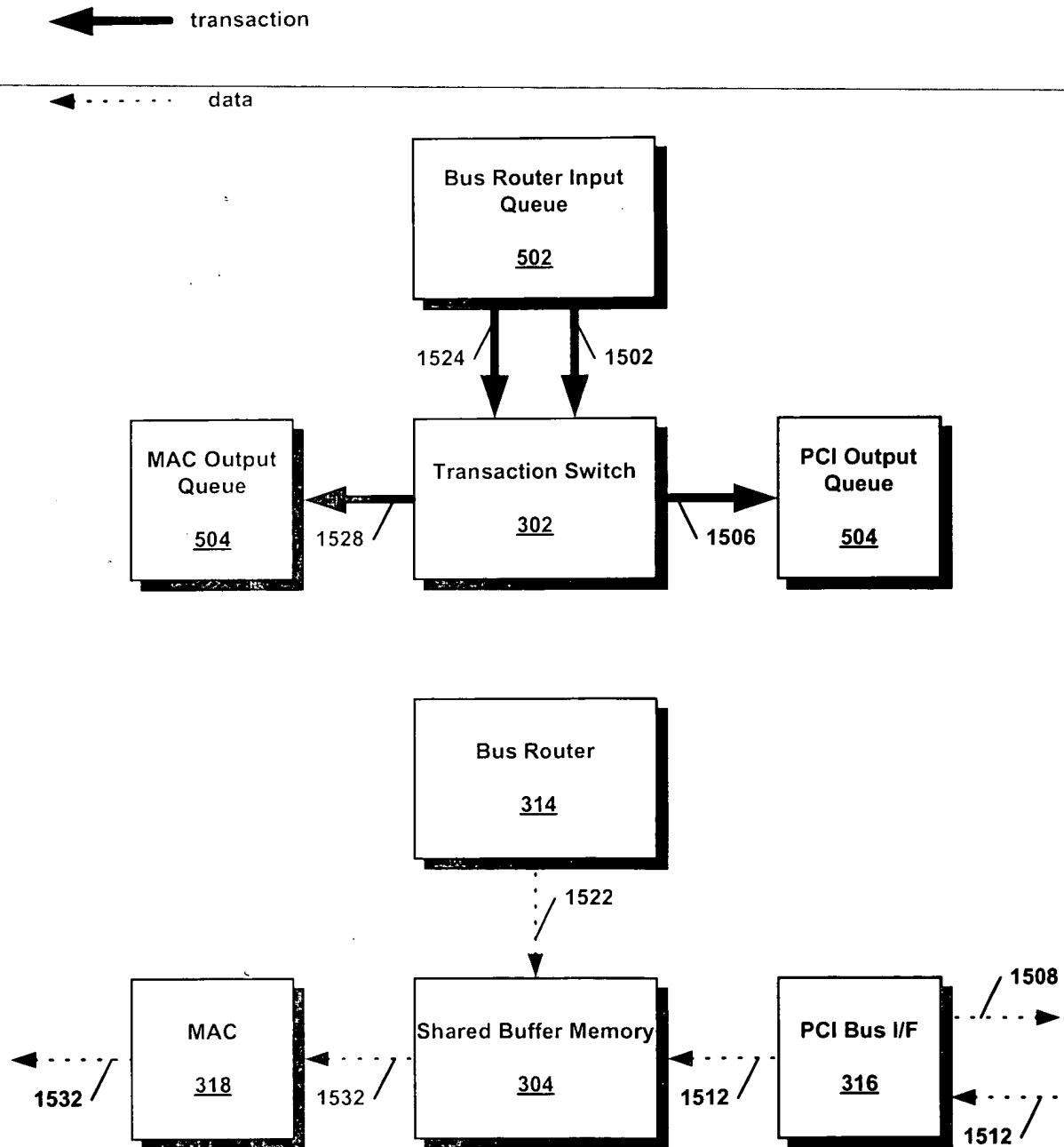
Packetized Data to Addressed Data Operation

FIG. 15a



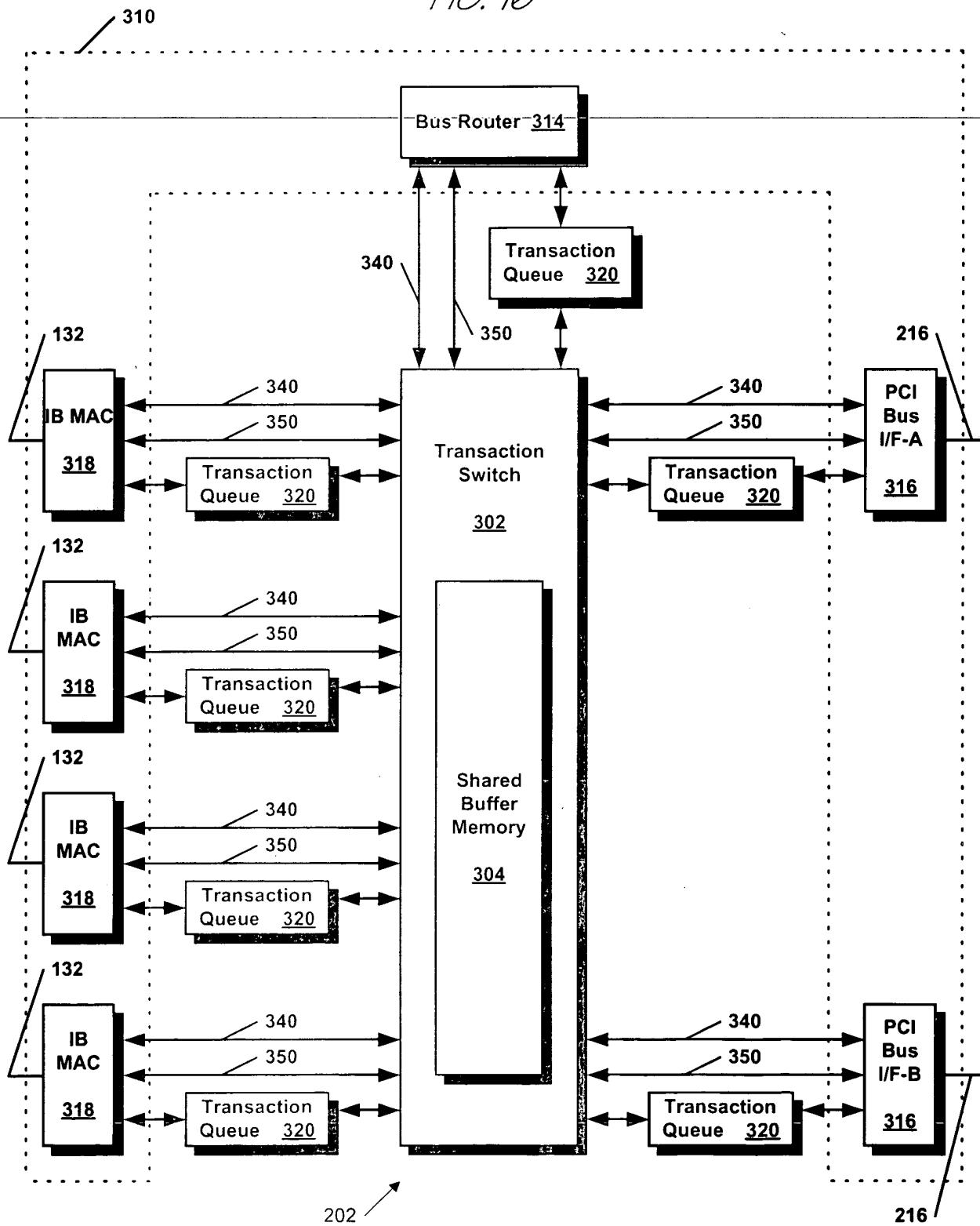
Addressed Data to Packetized Data Operation

FIG. 15b



Addressed Data to Packetized Data Operation

FIG. 16



IB Hybrid CA/Switch with Transaction Switch and Shared Buffer Memory

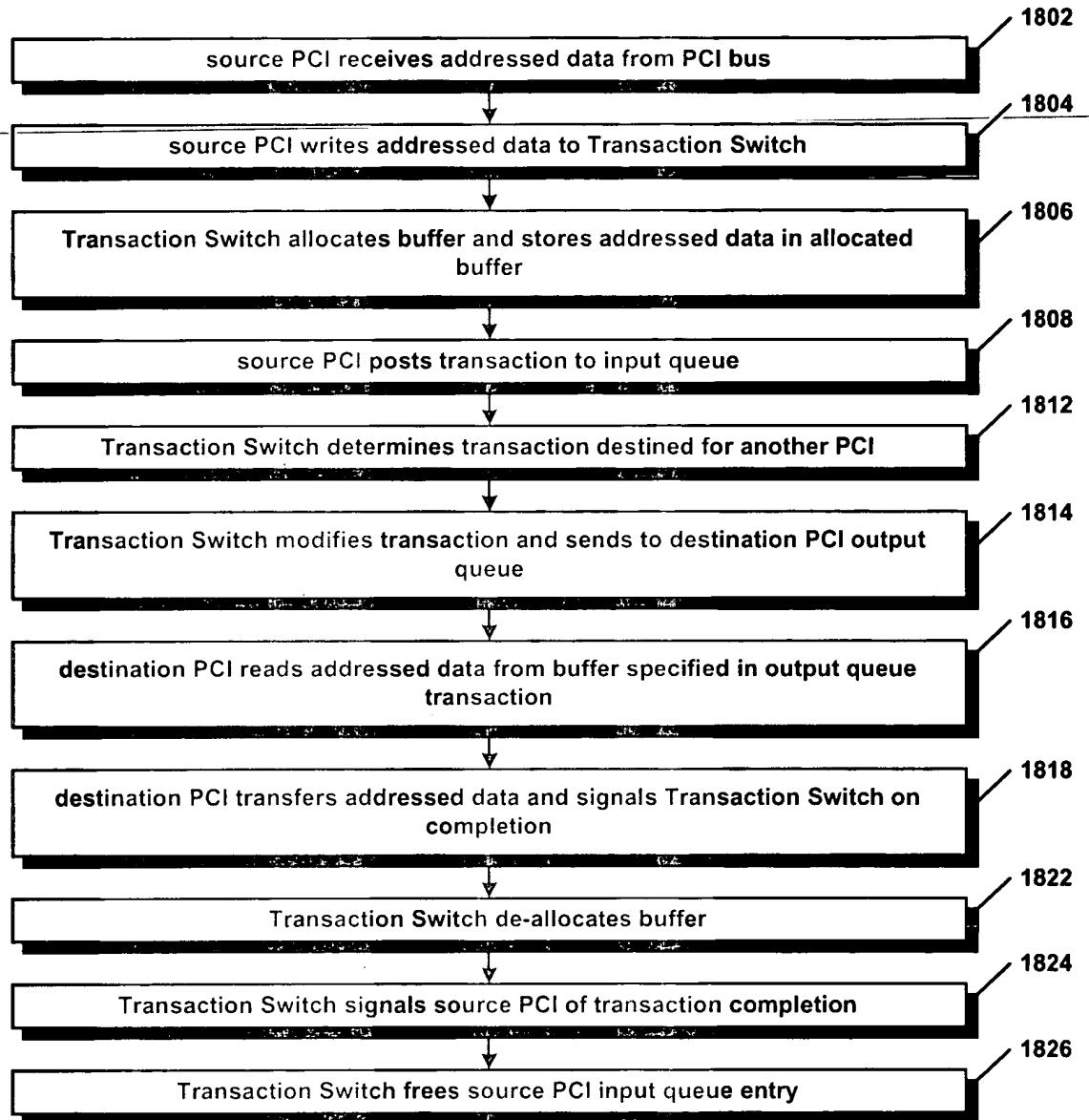
FIG. 17

PCI Address	Length	Buffer Address	PCI Cycle Type
<u>1702</u>	<u>1704</u>	<u>1706</u>	<u>1708</u>

PCI Input Queue Entry

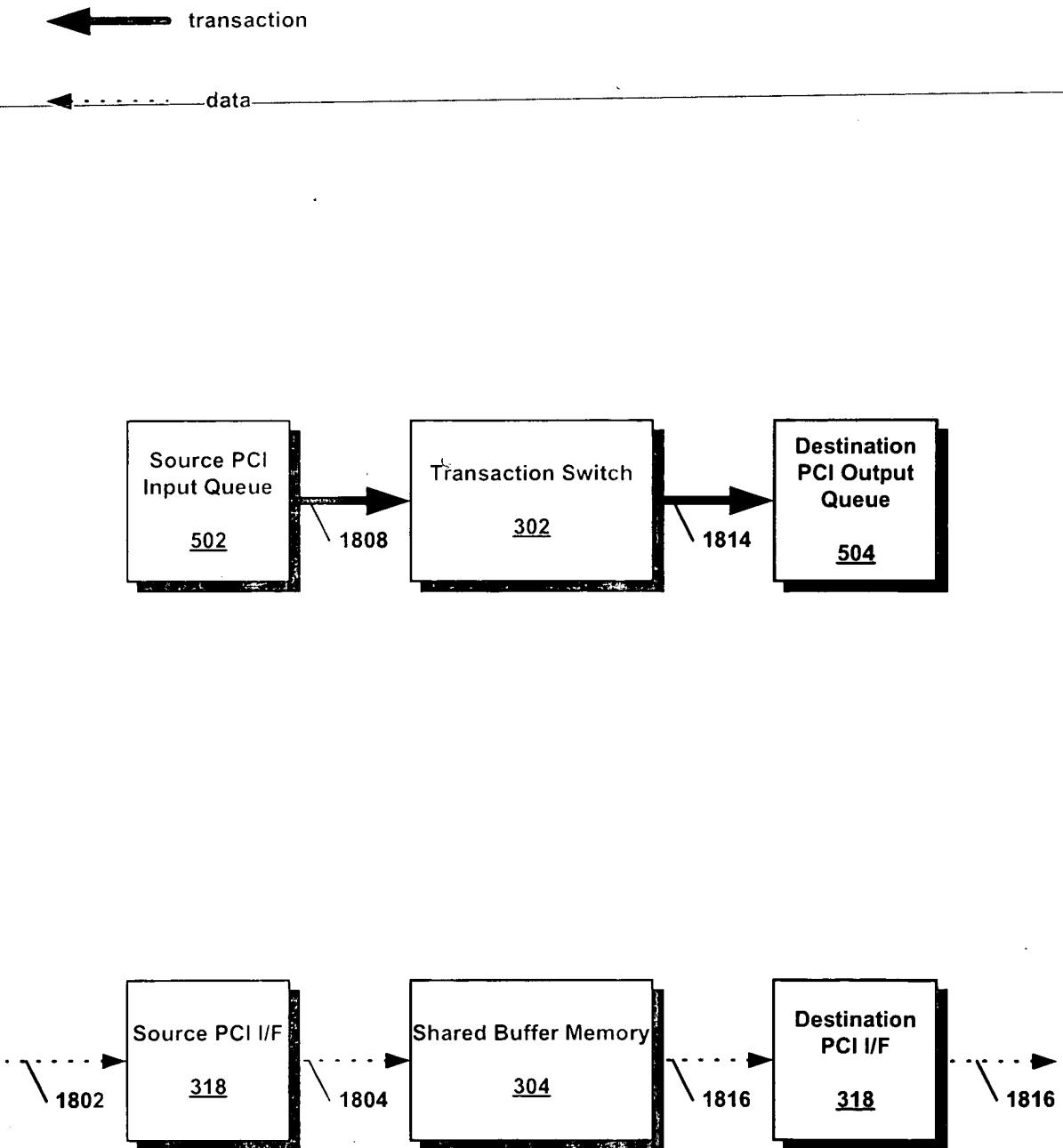
1700

FIG. 18a



Addressed Data Switching Operation

FIG. 18b



Addressed Data Switching Operation